UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/810,053 | 03/26/2004 | Klaas Bult | 51550/LTR/B600 | 7909 |

23363 7590 11/30/2004

CHRISTIE, PARKER & HALE, LLP
PO BOX 7068
PASADENA, CA 91109-7068

| EXAMINER | |
|---|---|
| YOUNG, BRIAN K | |
| ART UNIT | PAPER NUMBER |
| 2819 | |

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/810,053 | BULT ET AL. | |
| | Examiner | Art Unit | |
| | Brian Young | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claim 1 is objected to because of the following informalities: claim 1 recites "complementary data decoders", however, only one decoder is shown in the drawings (fig. 9, 129) and the specification refers to " a decoder" (pg.5, des. fig.9). Appropriate correction is required.

2. Claim 1 rejected under 35 U.S.C. 101 as claiming the same invention as that of claim1 of prior U.S. Patent No. 6,714,150. This is a double patenting rejection.

Claim 1 of the instant application recites "A digital to analog converter (DAC) a first bias source having a comprising: potential of one polarity; polarity; a bistable latch biased by the sources, the latch having first and second complementary terminals; first and second complementary data decoders; means for alternately connecting one of the data decoders to the first bias source while the other data a second bias source having a potential of the other decoder floats; and first and second transfer switches coupling the first and second decoders to the first and second terminals, respectively, responsive to timing pulses".

Claim 1 of Patent Number 6,714, 150 recites;

What is claimed is:

1. A digital to analog converter (DAC) comprising:

a first bias source having a potential of one polarity;

a second bias source having a potential of the other polarity;

a bistable latch biased by the sources, the latch having first and second complementary terminals;

first and second complementary data decoders;

means for alternately connecting one of the data decoders to the first bias source while the other data decoder floats; and

first and second transfer switches coupling the first and second decoders to the first and second terminals, respectively, responsive to timing pulses.

They appear to be exactly the same.

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Louagie et al discloses (fig.1) a known layout of a cell with only one current source, a switching element is associated with this current source, however use of a different number of sources by cell is also foreseeable and needs to be taken in account. The switching element illustrated on FIG. 1 comprises two mirrored transistors 01 and 02 connected in parallel and the current source comprises a third transistor 03. The sources of transistors 01 and 02 are connected to the drain of transistor 03, this last having its own drain connected to a substrate ground link VSS of the matrix component.

The drains of transistors 01 and 02 are respectively to output terminals OUTN and OUTP. Complementary control signals CS and CS are applied to the gates of transistors 01 and 02 and a bias voltage BV is applied to the gate of transistor 03. The bias voltage BV is common to all cells of the matrix structure, it controls the value of the current fed by transistor 03 in the cell to which this transistor belongs. Control signals CS and CS are provided by a bistable trigger 04 having a data input D connected to an output of a cell decoder OS and a clock input C receiving a clock signal CLK common for all the cells in the converter. The cell decoder OS receives row and column controls from a matrix addressing logic for switching on the current source when required. As already known the matrix addressing logic when receiving a digital signal converts such a signal in row and column controls for switching on a number of current sources depending on the digital value of the received signal. As all the source output terminals OUTN and all the source output terminals OUTP are respectively connected together it is provided on a converter output terminal OUTN an analog signal summing up the currents provided by the output terminals OUTN of all the sources then switched on. In the same way there is also an analog signal at a converter output terminal OUTP summing up the currents provided by the output terminals OUTP of all the sources then switched on.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

***